CY10E494
CY100E494
CY101E494

CYPRESS SEMICONDUCTOR

16,384 x 4 ECL Static RAM

Features

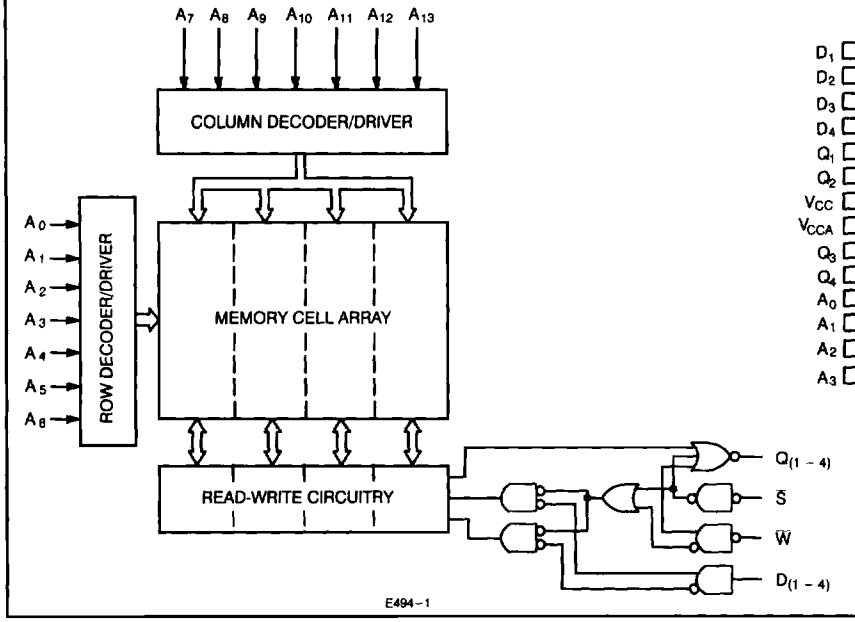
- **16,384 x 4 bits organization**
- **Ultra high speed/standard power**
  - t_{AA} = 7 ns
  - I_{EE} = 180 mA
- **Low-power version**
  - t_{AA} = 12 ns
  - I_{EE} = 135 mA
- **Both 10KH/10K- and 100K-compatible I/O versions as well as 100K with 10K supplies**
- **On-chip voltage compensation for improved noise margin**
- **Capable of withstanding >2001V ESD**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

Functional Description

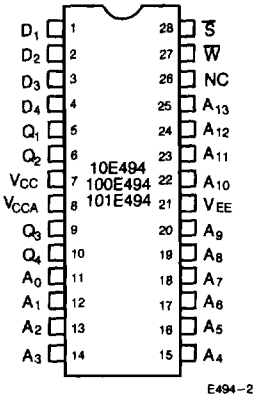
The Cypress CY10E494, CY100E494, and CY101E494 are 16K x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. Both parts are fully decoded random access memories organized as 16,384 words by 4 bits. The CY10E494 is 10KH/10K compatible, the CY100E494 is 100K compatible, and the CY101E494 has 100K-compatible levels with a −5.2V supply voltage.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memoryexpansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at $D_{(1-4)}$ is written into the addressed location. To read, $\overline{W}$ is held HIGH while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory.

Logic Block Diagram



Pin Configurations



Selection Guide

		10E494-7 101E494-7	10E494-8 100E494-8 101E494-8	10E494-10 100E494-10 101E494-10	10E494-12 100E494-12 101E494-12
Maximum Access Time (ns)		7	8	10	12
Maximum, I_{EE} (mA)	Commercial	180	180	180	
	L				135
	Military (10K/10KH only)			190	190

Shaded area contains preliminary information.

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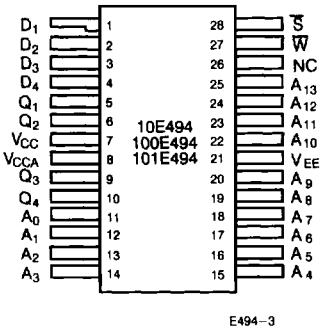
Pin Configurations (continued)

Rectangular Cerpak
Top View



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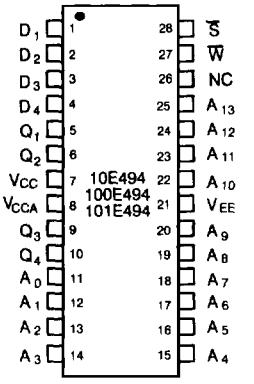
SOJ
Top View



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Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage V_{EE} to V_{CC} ..... − 7.0V to +0.5V

Input Voltage ..... V_{EE} to + 0.5V

Output Current ..... −50 mA

Static Discharge Voltage (per MIL−STD−883C, Method 3015) ..... > 2001V

Operating Range Referenced to V_{CC}

Range	Version	Ambient Temperature	V_{CC}
Commercial	10E	0°C to + 75°C	−5.2V ± 5%
Commercial	100E	0°C to + 85°C	−4.5V ± 0.3V
Commercial	101E	0°C to + 75°C	−5.2V ± 5%
Military	10E	− 55°C to + 125°C Case	−5.2V ± 5%

Shaded area contains preliminary information.

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Temperature[1]	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50Ω to − 2V V_{EE} = −5.2V, V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = − 55°C	−1140	−900	mV
			T_A = 0°C	−1000	−840	mV
			T_A = +25°C	−960	−810	mV
			T_A = +75°C	−900	−735	mV
			T_C = +125°C	−880	−700	mV
		100E R_L = 50Ω to − 2V, V_{EE} = −4.5V, 101E[3] V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1025	−880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50Ω to − 2V V_{EE} = − 5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = − 55°C	−1920	−1670	mV
			T_A = 0°C	−1870	−1665	mV
			T_A = +25°C	−1850	−1650	mV
			T_A = +75°C	−1830	−1625	mV
			T_C = +125°C	−1830	−1610	mV
		100E R_L = 50Ω to − 2V, V_{EE} = − 4.5V, 101E[3] V_{EE} = − 5.2V, V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1810	−1620	mV

Notes:

1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
2. 10E specifications support both 10K and 10KH compatibility.
3. 101E specifications support 100K compatibility with V_{EE} = −5.2V, T_A = 0°C to 75°C.

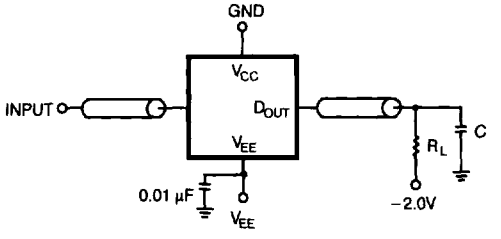
Electrical Characteristics Over the Operating Range (continued)

Parameters	Description	Test Conditions	Temperature[1]	Min.	Max.	Units
V_{IH}	Input HIGH Voltage	10E V_{EE} = − 5.2V	T_C = − 55°C	−1260	−900	mV
			T_A = 0°C	−1170	−840	mV
			T_A = +25°C	−1130	−810	mV
			T_A = +75°C	−1070	−720	mV
			T_C = +125°C	−1030	−700	mV
		100E V_{EE} = −4.5V 101E[3] V_{EE} = −5.2V	T_A = 0°C to 85°C	−1165	−880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = − 5.2V	T_C = − 55°C	−1950	−1540	mV
			T_A = 0°C	−1950	−1480	mV
			T_A = +25°C	−1950	−1475	mV
			T_A = +75°C	−1950	−1450	mV
			T_C = +125°C	−1950	−1450	mV
		100E V_{EE} = −4.5V 101E[3] V_{EE} = −5.2V	T_A = 0°C to 85°C	−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	S	0.5	170	µA
			All others	−50		
I_{EE}	Supply Current (All inputs and outputs open)	Commercial L (Low Power)		−135		mA
		Commercial Standard		−180		mA
		Military Standard		−190		mA

Capacitance[4]

Parameters	Description	Typ.	Max.[5]	Units
C_{IN}	Input Pin Capacitance	3	6	pF
C_{OUT}	Output Pin Capacitance	5	7	pF

AC Test Loads and Waveforms[6, 7, 8, 9, 10, 11]



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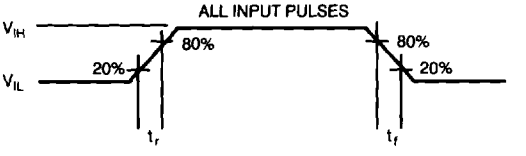

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Notes:

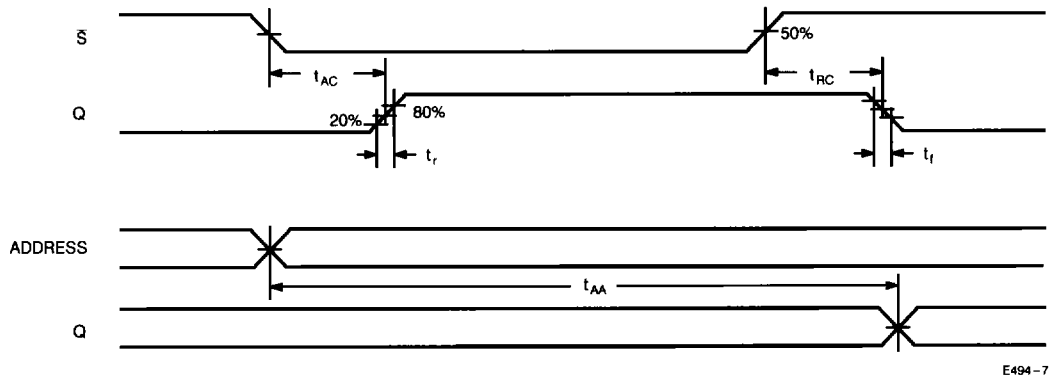
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except CerDIP (D42), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.
6. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
7. V_{IL} = −1.7V, V_{IH} = −0.9V on 100K version.
8. R_L = 50Ω C < 5 pF (7-, 8-ns grade) or < 30 pF (10-, 12-ns grade). Includes fixture and stray capacitance.
9. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
10. t_r = t_f = 0.7 ns.
11. All timing measurements are made from the 50% point of all waveforms.

Switching Characteristics Over the Operating Range

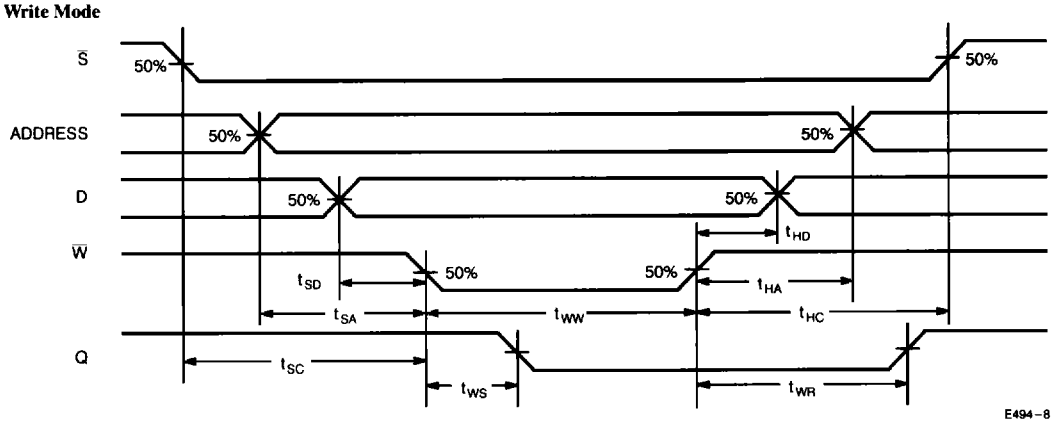
Parameters	Description	10E494–7 101E494–7		10E494–8 100E494–8 101E494–8		10E494–10 100E494–10 101E494–10		10E494–12 100E494–12 101E494–12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay		5.0		5.0		5.0		5.0	ns
t_{RC}	Chip Select Recovery		5.0		5.0		5.0		5.0	ns
t_{AA}	Address Access Time		7.0		8.0		10.0		12.0	ns
t_{WW}	Write Pulse Width	5.0		6.0		6.0		8.0		ns
t_{SD}	Data Set-Up to Write	1.0		1.0		2.0		2.0		ns
t_{HD}	Data Hold to Write	1.0		1.0		2.0		2.0		ns
t_{SA}	Address Set-Up/Write	1.0		1.0		2.0		2.0		ns
t_{HA}	Address Hold/Write	1.0		1.0		2.0		2.0		ns
t_{SC}	Chip Select Set-Up/Write	1.0		1.0		2.0		2.0		ns
t_{HC}	Chip Select Hold/Write	1.0		1.0		2.0		2.0		ns
t_{WS}	Write Disable		5.0		5.0		5.0		5.0	ns
t_{WR}	Write Recovery		8.0		8.0		12.0		14.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	1.5	0.35	1.5	0.75	2.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	1.5	0.35	1.5	0.75	2.5	ns

Switching Waveforms

Read Mode



Write Mode



Truth Table

Inputs			Output	
$\overline{S}$	$\overline{W}$	$\overline{D}$	Q	Mode
H	X	X	L	Disabled
L	L	H	L	Write H
L	L	L	L	Write L
L	H	X	D_{OUT}	Read

CYPRESS SEMICONDUCTOR

Ordering Information

Version	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Type	Operating Range
10E	180	7	CY10E494–7DC	D42	Commercial
			CY10E494–7KC	K80	
			CY10E494–7VC	V21	
		8	CY10E494–8DC	D42	
			CY10E494–8KC	K80	
			CY10E494–8VC	V21	
		10	CY10E494–10DC	D42	
			CY10E494–10KC	K80	
			CY10E494–10VC	V21	
	135	12	CY10E494L–12DC	D42	
			CY10E494L–12KC	K80	
			CY10E494L–12VC	V21	
	190	10	CY10E494–10DMB	D42	Military
			CY10E494–10KMB	K80	
		12	CY10E494–12DMB	D42	
			CY10E494–12KMB	K80	
100E	180	8	CY100E494–8DC	D42	Commercial
			CY100E494–8KC	K80	
			CY100E494–8VC	V21	
		10	CY100E494–10DC	D42	
			CY100E494–10KC	K80	
			CY100E494–10VC	V21	
	135	12	CY100E494L–12DC	D42	
			CY100E494L–12VC	V21	
			CY100E494L–12KC	K80	
101E	180	7	CY101E494–7DC	D42	Commercial
			CY101E494–7KC	K80	
			CY101E494–7VC	V21	
		8	CY101E494–8DC	D42	
			CY101E494–8KC	K80	
			CY101E494–8VC	V21	
		10	CY101E494–10DC	D42	
			CY101E494–10KC	K80	
			CY101E494–10VC	V21	
	135	12	CY101E494L–12DC	D42	
			CY101E494L–12KC	K80	
			CY101E494L–12VC	V21	

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Document #: 38–A–00009–C